

## ***Amendments to the Specification***

Please amend the table on page 1 of the disclosure as follows:

Docket #	Serial #	Title
CNTR:2021	<u>09/849736</u>	SPECULATIVE BRANCH TARGET ADDRESS CACHE
CNTR:2022	<u>09/849658</u>	APPARATUS, SYSTEM AND METHOD FOR DETECTING AND CORRECTING ERRONEOUS SPECULATIVE BRANCH TARGET ADDRESS CACHE BRANCHES
CNTR:2050	<u>09/849822</u>	DUAL CALL/RETURN STACK BRANCH PREDICTION SYSTEM
CNTR:2052	<u>09/849799</u>	SPECULATIVE BRANCH TARGET ADDRESS CACHE WITH SELECTIVE OVERRIDE BY SECONDARY PREDICTOR BASED ON BRANCH INSTRUCTION TYPE
CNTR:2062	<u>09/849754</u>	APPARATUS AND METHOD FOR SELECTING ONE OF MULTIPLE TARGET ADDRESSES STORED IN A SPECULATIVE BRANCH TARGET ADDRESS CACHE PER INSTRUCTION CACHE LINE
CNTR:2063	<u>09/849800</u>	APPARATUS AND METHOD FOR TARGET ADDRESS REPLACEMENT IN SPECULATIVE BRANCH TARGET ADDRESS CACHE

Please amend paragraph 87 on page 37 of the disclosure as follows:

The non-speculative branch direction predictor 412 generates a non-speculative prediction of the direction of a branch instruction 444, i.e., whether the branch will be taken or not taken, in response to the instruction decode information 492 received from the instruction decode logic 436. Preferably, the non-speculative branch direction predictor 412 includes one or more branch history tables for storing a history of resolved directions of executed branch instructions. Preferably, the branch history tables are used in conjunction with decode information of the branch instruction itself provided by the instruction decode logic 436 to predict a direction of conditional branch instructions. An exemplary embodiment of the non-speculative branch direction predictor 412 is described in U.S. Patent No. 6,550,004 entitled application serial number 09/434,984 (Docket Number CNTR:1498) — HYBRID BRANCH PREDICTOR WITH IMPROVED

SELECTOR TABLE UPDATE MECHANISM, having a common assignee and which is hereby incorporated by reference. Logic that ultimately resolves the direction of the branch instruction preferably resides in the E-stage 326 of the pipeline 300.

Please amend paragraph 90 on page 39 of the disclosure as follows:

An exemplary embodiment of the non-speculative call/return stack 414 is described in U.S. Patent No. 6,314,514 entitled application serial number 09/271,591 (Docket Number CNTR:1500)—METHOD AND APPARATUS FOR CORRECTING AN INTERNAL CALL/RETURN STACK IN A MICROPROCESSOR THAT SPECULATIVELY EXECUTES CALL AND RETURN INSTRUCTIONS, having a common assignee and which is hereby incorporated by reference.

Please amend paragraph 91 on page 39 of the disclosure as follows:

The non-speculative target address calculator 416 generates the non-speculative target address 354 of Figure 3 in response to the instruction decode information 492 received from the instruction decode logic 436. Preferably, the non-speculative target address calculator 416 includes an arithmetic logic unit for calculating a branch target address of PC-relative or direct type branch instructions. Preferably, the arithmetic logic unit adds an instruction pointer and length of the branch instruction to a signed offset comprised in the branch instruction to calculate the target address of PC-relative type branch instructions. Preferably, the non-speculative target address calculator 416 includes a relatively small branch target buffer (BTB) for caching branch target addresses of indirect type branch instructions. An exemplary embodiment of the non-speculative target address calculator 416 is described in U.S. Patent No. 6,609,194 entitled application serial number 09/438,907 (Docket Number CNTR:1507)—APPARATUS FOR PERFORMING BRANCH TARGET ADDRESS CALCULATION BASED ON BRANCH TYPE, having a common assignee and which is hereby incorporated by reference.

## **Remarks**

In the Office Action, the Examiner noted that claims 1-45 are pending in the application, and that claims 1-45 are rejected. By this amendment, claim 22 has been canceled, and claims 1 and 23 have been amended. Thus, claims 1-21 and 23-45 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

## ***In the Oath/Declaration***

Applicant notes the Examiner's indication that the declaration as originally submitted is defective because the title reflected in the declaration does not match the title in the specification. Applicant will submit a supplement declaration with the proper title on indication of allowable subject matter.

## ***In the Specification***

The Examiner objected to the form of the claims citing MPEP § 608.01(m) which states that the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). Applicant respectfully notes that the last text on page 113 of the specification, which immediately precedes the claims, reads "We claim:". Applicant does not understand MPEP § 608.01(m) to require each claim individually to begin with "We claim."

The specification has also been amended to fill in the serial numbers of the co-pending applications in the table on page 1. The specification has also been amended to insert the patent numbers of issued U.S. patents incorporated by reference in the specification.

## ***In the Claims***

### **Rejection Under 35 USC 102(b)**

The Examiner rejected claims 22, and 37-39 under 35 U.S.C. § 102(b), as being anticipated by *Emma et al.*, U.S. Patent No. 5,353,421A (hereinafter *Emma*). Claim 22 has been canceled. Applicant respectfully traverses the rejection of claims 37-39.

Generally speaking, *Emma* teaches a two-phase branch prediction mechanism. First, during an instruction fetch phase, a branch history table (BHT) predicts an outcome and target address of a branch instruction present in a cache segment in a cache specified by a fetch address. The BHT stores addresses of recently executed branch instructions, target addresses of the branch instructions, and a taken/not taken prediction of the branch instruction. If the fetch address hits in the BHT and the BHT predicts a branch instruction in the cache segment is taken, then the next fetch address is the target address predicted by the BHT, i.e., the processor branches to the target address predicted by the BHT. Second, during an instruction decode phase when the branch instruction reaches instruction decode logic that determines the instruction is a branch instruction, a decode history table (DHT) predicts an outcome of the branch instruction based on a portion of the current instruction address. The current instruction address is the address of the instruction currently being decoded, which may be a branch instruction. The DHT stores indications of whether conditional branch instructions specified by a portion of the current instruction address were taken or not taken in a previous execution thereof. If the DHT prediction disagrees with the BHT prediction, the BHT prediction may be subsequently overridden by the DHT prediction based on a predetermined set of rules.

With respect to claim 37, the Examiner asserts that *Emma* teaches generating a plurality of speculative branch direction predictions of an instruction prior to decoding the instruction. Applicant can find no teaching in *Emma* of generating a plurality of speculative branch direction predictions of an instruction prior to decoding the instruction, as recited by claim 37. *Emma*'s BHT generates a plurality of branch direction predictions for a corresponding plurality of branch instructions that may be present in the cache segment selected by the fetch address, not a plurality of branch direction predictions for the same branch instruction. See col. 12, line 62 to col. 13, line 3; col. 13, lines 25-28. Furthermore, although the BHT and DHT each generate a direction prediction (a plurality) potentially for the same branch instruction, the DHT does not generate its direction prediction prior to decoding the branch instruction. Therefore, *Emma* does not anticipate claim 37.

Applicant respectfully asserts *Emma* does not anticipate dependent claims 38-39 because they depend from independent claim 37, which is not anticipated by *Emma* for the reasons discussed above.

### **Rejection Under 35 USC 103**

The Examiner rejected claims 1-11 under 35 U.S.C. § 103 as being unpatentable over *Emma* in view of *McFarling* (“WRL Technical Note TN-36, Combining Branch Predictors,” Digital Equipment Corp., 1993) (hereinafter *McFarling*). Applicant respectfully traverses the Examiner’s rejections.

With respect to claim 1, the Examiner asserts that *Emma* teaches logic (Gate “G” of Fig. 6) that provides a binary function of the fetch address on an output. Applicant respectfully asserts that *Emma*’s Gate G does not provide a binary function of a fetch address. *Emma*’s Gate G provides a portion of the current instruction address (element 26 of Figs. 4 and 6), not *Emma*’s instruction cache fetch address shown as the FETCH REQUEST AND ADDRESS input to cache 13 of Fig. 10, i.e., the address at which instructions are fetched from the cache. Rather, the current instruction address is the address of the current instruction being decoded (which may be a branch instruction), see col. 14, lines 56-60, not an instruction cache fetch address. Thus, *Emma*’s DHT is indexed by a portion of the current instruction address, not by a function of the fetch address. Therefore, *Emma*’s Gate G does not teach logic that provides a binary function of the fetch address on an output and *Emma*’s DHT does not predict whether a branch instruction will be taken based on a binary function of the fetch address.

Further with respect to claim 1, the Examiner asserts that *Emma* inherently teaches a selector for selecting one of first and second predictors based on a fetch address, citing Fig. 13. Applicant respectfully asserts that *Emma* does not teach a selector for selecting one of first and second predictors based on a fetch address. Fig. 13 teaches comparison logic that compares a branch instruction address (not a fetch address) from the instruction decoder with a branch instruction address (not a fetch address) from a stack that stores branch address/target address pairs provided by the BHT. As discussed above with respect to the current instruction address, *Emma*’s branch instruction addresses are

addresses of a particular instruction, namely of the branch instruction in question, not the address of a cache segment that may contain the branch instruction, i.e., the fetch address. Thus, *Emma*'s Fig. 13 does not teach a selector for selecting one of first and second predictors based on a fetch address.

Still further with respect to claim 1, Applicant has amended claim 1 to clarify that the first and second predictors predict in parallel whether the branch instruction will be taken or not taken based on the fetch address. In contrast, *Emma* specifically teaches that the BHT and DHT make their predictions of whether a particular branch instruction will be taken or not taken at different times, i.e., sequentially, namely the BHT at instruction fetch time and the DHT at instruction decode time. See col. 17, lines 12-17; Abstract; col. 4, lines 15-19; and claim 8. Therefore, *Emma* does not teach first and second predictors predicting in parallel whether a branch instruction will be taken or not taken based on a fetch address.

Finally with respect to claim 1, *McFarling* teaches indexing his branch history tables with a program counter (PC), which is analogous to the current instruction address of *Emma*, not indexing the branch history tables with a fetch address. As the Examiner states, *McFarling* teaches making branch predictions using branch instruction addresses, which as discussed above are not cache fetch addresses. Furthermore, Applicant can find no teaching in *McFarling* of making branch predictions based on a cache fetch address. Predicting branch instructions using a cache fetch address is quite different from predicting branch instructions using a program counter, since typically the first is performed before the instruction is decoded and the second is performed after the instruction is decoded. Consequently, Applicant can find no teaching, suggestion, or motivation to combine the teachings of *Emma* and *McFarling* at the time Applicant made his invention. For each of the reasons stated above, Applicant respectfully asserts that *Emma* in view of *McFarling* does not obviate claim 1.

Applicant respectfully asserts *Emma* in view of *McFarling* does not obviate dependent claims 2-11 because they depend from independent claim 1, which is not obviated by *Emma* in view of *McFarling* for the reasons discussed above.

The Examiner rejected claims 12-21, 23, 24, 30-36, and 40-44 under 35 U.S.C. § 103 as being unpatentable over *Black et al.*, U.S. Patent No. 5,761,723A (hereinafter *Black*) in view of *McFarling*. Applicant respectfully traverses the Examiner's rejections.

First, Applicant notes that predicting a branch instruction requires two components: (1) the direction prediction, which is a prediction of whether the branch instruction will be taken or not taken, and (2) the branch target address, which is a prediction of the address to which the branch instruction will branch if taken. The direction prediction is distinct from the target address, as Applicant's specification describes throughout. See, for example, the second sentence of paragraph 10 on Page 6. *Black* also teaches the direction of a branch instruction is whether the branch is taken or not taken. See col. 7, lines 11-32.

Generally speaking, *Black* teaches an instruction cache that provides instructions in response to a fetch address. *Black* also teaches a branch target address cache (BTAC) that stores target addresses of recently taken branch instructions paired with the fetch address used to fetch the branch instructions from the instruction cache. The fetch address is also provided to the BTAC, which compares the fetch address with the fetch addresses stored therein. If the fetch address matches a fetch address stored in the BTAC, the BTAC provides the target address associated with the matching fetch address and asserts a HIT/MISS signal to indicate the match. *Black* also teaches a multiplexer that receives the BTAC target address along with other addresses, such as a sequential address that is the current fetch address updated according to the number of instructions fetched in the current clock cycle, and selects one of the addresses as the next fetch address to be provided to the instruction cache and BTAC. This enables the processor to selectively execute instructions sequentially or to branch to other addresses. If the BTAC asserts the HIT/MISS signal, the multiplexer selects the BTAC target address, unless a higher priority source indicates its address should be selected according to a fixed priority scheme wherein later stages have priority over earlier stages in order to correct earlier predictions. In some circumstances, such as after a context switch, the BTAC may assert the HIT/MISS signal even though no branch instruction is present in the instructions specified by the fetch address, which *Black* refers to as a "phantom branch."

*Black* also teaches a branch history table (BHT) that stores a history state for each recently encountered branch instruction. The BHT also receives the instruction cache fetch address and provides the history state indexed by the fetch address to a decode buffer. The decode buffer also receives instructions from the instruction cache. During a clock cycle subsequent to the clock cycle in which the BTAC provides its target address and HIT/MISS signal, the decode buffer provides an instruction, such as a branch instruction, and the history state to decode prediction logic. When the decode prediction logic decodes a branch instruction, the decode prediction logic uses the history state provided by the BHT to predict whether the conditional branch instruction will be taken or not taken. The decode prediction logic also generates the target address of the branch instruction specified by the branch instruction itself and provides the target address to the multiplexer. If the decode prediction logic determines from the history state that the BHT predicts the branch instruction will be taken, the decode prediction logic asserts a DECODE CORRECTION signal, in response to which the multiplexer selects the target address provided by the decode prediction logic, unless a higher priority source indicates its address should be selected.

With respect to claim 12, the Examiner asserted that *Black* teaches a multiplexer for selecting one of first and second direction predictions based on a selection signal, citing the fetch address selection multiplexer. Applicant respectfully asserts that *Black*'s fetch address multiplexer does not select a direction prediction, but instead selects a next fetch address from one of multiple addresses, such as a branch target address provided by the BTAC or by the decode prediction logic. As discussed above, a branch target address is not a direction prediction, i.e., a prediction of whether a branch instruction will be taken or not taken. Additionally, Applicant can find no teaching or suggestion to combine the teachings of *Black* and *McFarling* at the time Applicant made his invention. For each the reasons stated above, Applicant respectfully asserts that *Black* in view of *McFarling* does not obviate claim 12.

Applicant respectfully asserts *Black* in view of *McFarling* does not obviate dependent claims 13-21 because they depend from independent claim 12, which is not obviated by *Black* in view of *McFarling* for the reasons discussed above.

With respect to claim 23, the Examiner asserts that *Black* teaches control logic for causing a microprocessor to speculatively branch if one of first and second predictions selected by a selector provided by a BTAC predicts that a branch instruction presumed present in an instruction cache line selected by a fetch address will be taken. Applicant has amended claim 23 to clarify that the control logic causes the microprocessor to branch prior to the branch instruction being decoded. Applicant respectfully asserts that *Black* does not teach control logic for causing a microprocessor to speculatively branch, prior to decode of the branch instruction, if one of the first and second predictions selected by the selector predicts that the branch instruction will be taken as recited in amended claim 23. As discussed above with respect to claim 12, although *Black*'s BHT provides history state prior to decode of the branch instruction, the history state is not used to make a prediction until after the branch instruction is decoded by the decode prediction logic to determine that a branch instruction is actually present. In particular, the decode prediction logic must determine whether the branch instruction is a conditional or unconditional branch and must determine the target address from the branch instruction itself before it can use the BHT history state to branch the microprocessor. Additionally, Applicant can find no teaching or suggestion to combine the teachings of *Black* and *McFarling* at the time Applicant made his invention. For each the reasons stated above, Applicant respectfully asserts that *Black* in view of *McFarling* does not obviate claim 23.

Applicant respectfully asserts *Black* in view of *McFarling* does not obviate dependent claims 24-36 because they depend from independent claim 23, which is not obviated by *Black* in view of *McFarling* for the reasons discussed above.

With respect to claim 40, the Examiner asserts that *Black* teaches generating a first prediction of whether a branch instruction will be taken, citing the history state output by the BHT as the first prediction. The Examiner also asserts that *Black* teaches selecting one of the first prediction and a second prediction as a final prediction, citing the DECODE CORRECTION signal output by the decode prediction logic as the first prediction. Applicant respectfully asserts that the BHT history state and the DECODE CORRECTION signal cannot both be the first prediction recited in claim 40, as the

Examiner appears to assert. Applicant respectfully asserts that neither the BHT history state nor the DECODE CORRECTION signal satisfy the required limitations recited in claim 40. Although the BHT history state is generated before it is known whether the instruction being fetched is a branch or not, it is not provided to the address selector and fetch address multiplexer, which the Examiner recites as performing the selecting one of first and second predictions as a final prediction step of claim 40. Conversely, although the DECODE CORRECTION signal is provided to the address selector and fetch address multiplexer, the DECODE CORRECTION signal is generated after the branch instruction is decoded by the decode prediction logic. Furthermore, as discussed above with respect to claim 12, *Black*'s fetch address multiplexer selects branch target address predictions, not branch direction predictions, i.e., predictions of whether the branch instruction will be taken or not taken. Additionally, Applicant can find no teaching or suggestion to combine the teachings of *Black* and *McFarling* at the time Applicant made his invention. For each the reasons stated above, Applicant respectfully asserts that *Black* in view of *McFarling* does not obviate claim 40.

Applicant respectfully asserts *Black* in view of *McFarling* does not obviate dependent claims 41-45 because they depend from independent claim 40, which is not obviated by *Black* in view of *McFarling* for the reasons discussed above.

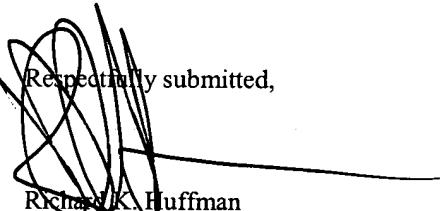
The Examiner has indicated additional prior art which is made of record and not relied upon. None of these references anticipate or obviate applicant's invention.

For all of the reasons advanced above, Applicant respectfully submits that claims 1-21 and 23-45 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

For all of the reasons advanced above, Applicant respectfully submits that claims 1-21 and 23-45 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

  
Respectfully submitted,

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Date: 6/1/2004

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By: Richard K. Huffman